WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a first memory cell block which includes:

a plurality of first memory cells each of which includes a cell transistor having a gate terminal connected to a word line and ferroelectric capacitor connected at one end to a source terminal of the cell transistor,

a first reset transistor having a source terminal connected to a first plate line and a drain terminal connected to a first local bit line with drain terminals of the cell transistors of the first memory cells used as the first local bit line and each of the other end of the ferroelectric capacitors used as the first plate line, and

a first block selection transistor having a source terminal connected to the first local bit line and a drain terminal connected to a first bit line.

2. The device according to claim 1, wherein the cell transistors are ON in a standby time and the cell transistors other than the cell transistor of selected one of the first memory cells are OFF in an active time.

3. The device according to claim 2, wherein the first reset transistor is ON and the first block selection transistor is OFF in the standby time.

4. The device according to claim 1, wherein the first plate line is at ground potential in a standby time and potential of the word lines of non-selected ones of the first memory cells are lower than potential of the word line of a selected one of the first memory cells in an active time.

5. The device according to claim 1, wherein potential of the first plate line is higher than ground potential in a standby time.

6. The device according to claim 1, wherein potential of the first plate line is driven from a low level to a high level and from the high level to the low level in an active time.

7. The device according to claim 1, wherein the first block selection transistor is ON in an active time.

8. The device according to claim 1, wherein the first local bit line is provided above the ferroelectric capacitor.

9. The device according to claim 1, wherein the first local bit line is provided below the ferroelectric capacitor.

10. The device according to claim 1, wherein the semiconductor integrated circuit device in claim 1 is formed on a semiconductor substrate and a logic circuit is formed on the semiconductor substrate.

11. The device according to claim 1, further

comprising a second memory cell block which includes:

a plurality of second memory cells each of which includes a cell transistor having a gate terminal connected to the word line and a ferroelectric capacitor connected at one end to a source terminal of the cell transistor of the second memory cell,

a second reset transistor having a source terminal connected to a second plate line and a drain terminal connected to a second local bit line with drain terminals of the cell transistors of the second memory cells used as the second local bit line and the other end of each of the ferroelectric capacitors used as the second plate line, and

a second block selection transistor having a source terminal connected to the second local bit line and a drain terminal connected to a second bit line,

wherein a first block selection signal supplied to a gate terminal of the first block selection transistor is different from a second block selection signal supplied to a gate terminal of the second block selection transistor.

12. The device according to claim 11, wherein the cell transistors are ON in a standby time and the cell transistors other than the cell transistor of selected one of the first memory cells are OFF in an active time.

13. The device according to claim 12, wherein the

first reset transistor is ON and the first block selection transistor is OFF in the standby time.

14. The device according to claim 11, wherein the first plate line is at ground potential in a standby time and potential of the word lines of non-selected ones of the first memory cells are lower than potential of the word line of a selected one of the first memory cells in an active time.

15. The device according to claim 11, wherein potential of the first plate line is higher than ground potential in a standby time.

16. The device according to claim 11, wherein potential of the first plate line is driven from a low level to a high level and from the high level to the low level in an active time.

17. The device according to claim 11, wherein potential of the first plate line or the second plate line is driven from a low level to a high level and from the high level to the low level in an active time.

18. The device according to claim 11, wherein the first block selection transistor or the second block selection transistors is ON in an active time.

19. The device according to claim 11, wherein the first local bit line and the second local bit line are provided above the ferroelectric capacitor.

20. The device according to claim 11, wherein the first local bit line and the second local bit line are

provided below the ferroelectric capacitor.

21. The device according to claim 11, wherein the semiconductor integrated circuit device in claim 11 is formed on a semiconductor substrate and a logic circuit is formed on the semiconductor substrate.

22. A semiconductor integrated circuit device comprising:

a first memory cell block which includes:

a plurality of first memory cells each of which includes a cell transistor having a gate terminal connected to a word line and a ferroelectric capacitor connected at one end to a source terminal of the cell transistor,

a first reset transistor having a source terminal connected to a first power supply and a drain terminal connected to a first local bit line with drain terminals of the cell transistors used as the first local bit line and the other end of each of the ferroelectric capacitors used as a first plate line, and

a first block selection transistor having a source terminal connected to the first local bit line and a drain terminal connected to a first bit line.

23. The device according to claim 22, wherein the cell transistors are ON in a standby time and the cell transistors other than the cell transistor of selected one of the first memory cells are OFF in an active

time.

24. The device according to claim 23, wherein the first reset transistor is ON and the first block selection transistor is OFF in the standby time.

25. The device according to claim 24, wherein potential of the first power supply is equal to potential of the first plate line in a standby time.

26. The device according to claim 22, wherein the first plate line is at ground potential in a standby time and potential of the word lines of non-selected ones of the first memory cells are lower than potential of the word line of a selected one of the first memory cells in an active time.

27. The device according to claim 22, wherein potential of the first plate line is higher than ground potential in a standby time.

28. The device according to claim 22, wherein potential of the first plate line is driven from a low level to a high level and from the high level to the low level in an active time.

29. The device according to claim 21, wherein the first block selection transistor is ON in an active time.

30. The device according to claim 22, wherein the first local bit line is provided above the ferroelectric capacitor.

31. The device according to claim 22, wherein

the first local bit line is provided below the ferroelectric capacitor.

32. The device according to claim 22, wherein the semiconductor integrated circuit device in claim 22 is formed on a semiconductor substrate and a logic circuit is formed on the semiconductor substrate.

33. The device according to claim 22, further comprising a second memory cell block which includes:

a plurality of second memory cells each of which includes a cell transistor having a gate terminal connected to the word line and a ferroelectric capacitor connected at one end to a source terminal of the cell transistor of the second memory cell,

a second reset transistor having a source terminal connected to the first power supply and a drain terminal connected to a second local bit line with drain terminals of the cell transistors of the second memory cells used as the second local bit line and the other end of each of the ferroelectric capacitors used as a second plate line, and

a second block selection transistor having a source terminal connected to the second local bit line and a drain terminal connected to a second bit line,

wherein a first block selection signal supplied to a gate terminal of the first block selection transistor is different from a second block selection signal supplied to a gate terminal of the second block

selection transistor.

34. The device according to claim 33, wherein the cell transistors are ON in a standby time and the cell transistors other than the cell transistor of selected one of the first memory cells are OFF in an active time.

35. The device according to claim 34, wherein the first reset transistor is ON and the first block selection transistor is OFF in the standby time.

36. The device according to claim 35, wherein potential of the first power supply is equal to potential of the first plate line in a standby time.

37. The device according to claim 33, wherein the first plate line is at ground potential in a standby time and potential of the word lines of non-selected ones of the first memory cells are lower than potential of the word line of a selected one of the first memory cells in an active time.

38. The device according to claim 33, wherein potential of the first plate line is higher than ground potential in a standby time.

39. The device according to claim 33, wherein potential of the first plate line is driven from a low level to a high level and from the high level to the low level in an active time.

40. The device according to claim 33, wherein potential of the first plate line or the second plate

line is driven from a low level to a high level and from the high level to the low level in an active time.

41. The device according to claim 33, wherein the first block selection transistor or the second block selection transistor is ON in an active time.

42. The device according to claim 33, wherein the first local bit line and the second local bit line are provided above the ferroelectric capacitor.

43. The device according to claim 33, wherein the first local bit line and the second local bit line are provided below the ferroelectric capacitor.

44. The device according to claim 33, wherein the semiconductor integrated circuit device in claim 33 is formed on a semiconductor substrate and a logic circuit is formed on the semiconductor substrate.

45. A semiconductor integrated circuit device comprising:

a memory cell array having a first memory block and a second memory cell block each of which includes:

a plurality of memory cells each of which includes a cell transistor having a gate terminal connected to a word line and a ferroelectric capacitor connected at one end to a source terminal of the cell transistor, and

a block selection transistor having a source terminal connected to a local bit line with drain terminals of the cell transistors used as the local bit

line and the other end of each of the ferroelectric capacitors used as a plate line,

wherein drain terminals of the block selection transistors of the first memory cell block and the second memory cell block are connected to a bit line,

the cell transistors and block selection transistors of the first memory cell block and the second memory cell block are ON in a standby time, and

the block selection transistor of the first memory cell block is OFF and the cell transistor of the memory cell other than one selected one of the memory cells in the first memory cell block is OFF in an active time.

46. The device according to claim 11, further comprising:

a first amplification transistor having a gate connected to the first local bit line, a drain connected to the second bit line and a source connected to a first power supply and

a second amplification transistor having a gate connected to the second local bit line, a drain connected to the first bit line and a source connected to the first power supply or a second power supply.

47. The device according to claim 46, wherein

first data is read out from a selected one of the first memory cells to the first local bit line by selecting the first plate line in an active time,

a first amplification signal generated by

amplifying the first data by use of the first amplification transistor is read out to the second bit line,

a second amplification signal complementary to the first amplification signal is supplied to the first bit line by amplifying the first amplification signal by use of a sense amplifier connected to the first bit line and the second bit line, and

the second amplification signal is supplied to the selected first memory cell via the first block selection transistor, the first data being rewritten into the selected first memory cell.

48. The device according to claim 33, further comprising:

a first amplification transistor having a gate connected to the first local bit line, a drain connected to the second bit line and a source connected to a first power supply and

a second amplification transistor having a gate connected to the second local bit line, a drain connected to the first bit line and a source connected to the first power supply or a second power supply.

49. The device according to claim 48, wherein

first data is read out from a selected one of the first memory cells to the first local bit line by selecting the first plate line in an active time,

a first amplification signal generated by

amplifying the first data by use of the first amplification transistor is read out to the second bit line,

a second amplification signal complementary to the first amplification signal is supplied to the first bit line by amplifying the first amplification signal by use of a sense amplifier connected to the first bit line and the second bit line, and

the second amplification signal is supplied to the selected first memory cell via the first block selection transistor, the first data being rewritten into the selected first memory cell.

50. The device according to claim 1, further comprising a second memory cell block which includes:

a plurality of second memory cells each of which includes a cell transistor having a gate terminal connected to the word line and a ferroelectric capacitor connected at one end to a source terminal of the cell transistor,

a second reset transistor having a source terminal connected to the first plate line and a drain terminal connected to a second local bit line with drain terminals of the cell transistors of the second memory cells used as the second local bit line, and

a second block selection transistor having a source terminal connected to the second local bit line and a drain terminal connected to a second bit line.

51. The device according to claim 50, wherein the cell transistors are ON in a standby time and the cell transistors other than the cell transistor of selected one of the first memory cells are OFF in an active time.

52. The device according to claim 50, wherein the first reset transistor and the second reset transistor are ON and the first block selection transistor and the second block selection transistor are OFF in a standby time.

53. The device according to claim 50, wherein adjacent two first memory cell blocks are connected to the first plate line.

54. The device according to claim 50, wherein the first local bit line and the second local bit line are provided above the ferroelectric capacitor.

55. The device according to claim 50, wherein the first local bit line and the second local bit line are provided below the ferroelectric capacitor.

56. The device according to claim 50, wherein the semiconductor integrated circuit device in claim 50 is formed on a semiconductor substrate and a logic circuit is formed on the semiconductor substrate.

57. A semiconductor integrated circuit device comprising:

a memory cell block which includes:

a plurality of memory cells each of which includes

a cell transistor having a gate terminal connected to a word line and a ferroelectric capacitor connected at one end to a source terminal of the cell transistor,

a reset transistor having a source terminal connected to a plate line and a drain terminal connected to a local bit line with drain terminals of the cell transistors used as the plate line and the other end of each of the ferroelectric capacitors used as the local bit line, and

a block selection transistor having a source terminal connected to the local bit line and a drain terminal connected to a bit line.

58. The device according to claim 57, wherein the cell transistors are ON in a standby time and the cell transistors other than the cell transistor of selected one of the memory cells are OFF in an active time.

59. The device according to claim 57, wherein the reset transistor is ON and the first block selection transistor is OFF in a standby time.

60. The device according to claim 57, wherein adjacent two memory cell blocks are connected to the plate line.

61. The device according to claim 57, wherein the local bit line is provided above the ferroelectric capacitor.

62. The device according to claim 57, wherein the local bit line is provided below the ferroelectric

capacitor.

63. The device according to claim 57, wherein the semiconductor integrated circuit device in claim 57 is formed on a semiconductor substrate and a logic circuit is formed on the semiconductor substrate.

64. A semiconductor integrated circuit device comprising:

a memory cell group including a plurality of memory cell units each of which includes:

a plurality of memory cells each of which includes a cell transistor having a gate terminal connected to a word line and a ferroelectric capacitor connected at one end to a source terminal of the cell transistor with the other end of the ferroelectric capacitor used as a first terminal and a drain of the cell transistor as a second terminal; and

a reset transistor having a source terminal connected to a third terminal and a drain terminal connected to a fourth terminal, one of the first terminal and the second terminal of the memory cells being connected to the third terminal and the other end being connected to the fourth terminal;

wherein the memory cell units are series-connected with the third terminal and the fourth terminal used as its two terminals.

65. The device according to claim 64, wherein one end of the memory cell group is connected to a plate

line and the other end is connected to a bit line via a memory cell group selection transistor.

66. The device according to claim 64, wherein the reset transistor of each of the memory cell units in the memory cell group are controlled by different signals.

67. The device according to claim 66, wherein

gates of the memory cell group selection transistors in two memory cell groups respectively connected to two bit lines forming a bit line pair are controlled by different signals, and

the plate lines in two memory cell groups are controlled by different signals.

68. The device according to claim 65, wherein all the cell transistors and all the reset transistors are ON and all the memory cell group selection transistors are OFF in a standby time.

69. The device according to claim 65, wherein in an active time in the selected memory cell group,

the cell transistors of the memory cells other than the selected memory cell and the memory cells connected to the word line of the selected memory cell are OFF,

the reset transistor of the memory cell unit including the selected memory cell is OFF,

the memory cell group selection transistor is ON, and

the plate line is driven.

70. The device according to claim 64, wherein a wiring connecting the first terminal of the memory cell to that of the other memory cell, and a wiring connecting the second terminal of the memory cell to that of the other memory cell are provided above the ferroelectric capacitor.

71. The device according to claim 64, wherein a wiring connecting the first terminal of the memory cell to that of the other memory cell, and a wiring connecting the second terminal of the memory cell to that of the other memory cell are provided below the ferroelectric capacitor.

72. The device according to claim 64, wherein the semiconductor integrated circuit device in claim 57 is formed on a semiconductor substrate and a logic circuit is formed on the semiconductor substrate.

73. A semiconductor integrated circuit device comprising:

a semiconductor substrate,

a plurality of cell transistors provided on a surface of the semiconductor substrate,

a local bit line provided above the cell transistors and electrically connected to one of a source diffusion layer and a drain diffusion layer of each of the cell transistors,

ferroelectric capacitors corresponding in number

to the cell transistors, provided above the local bit line, each of the ferroelectric capacitors has an upper electrode and a lower electrode electrically connected to the other one of the source diffusion layer and drain diffusion layer of corresponding one of the cell transistors,

a plate line provided above the upper electrodes and electrically connected to the upper electrodes,

a reset transistor provided on the surface of the semiconductor substrate with one of a source diffusion layer and a drain diffusion layer electrically connected to the plate line and the other one electrically connected to the local bit line, and

a block selection transistor provided on the surface of the semiconductor substrate with one of a source diffusion layer and a drain diffusion layer electrically connected to a bit line provided above the plate line and the other one electrically connected to the local bit line.

74. The device according to claim 73, wherein the source diffusion layer and the drain diffusion layer are different in a coordinate value on an axe extending along each of the gate electrodes of the cell transistors.

75. A semiconductor integrated circuit device comprising:

a semiconductor substrate,

a plurality of cell transistors provided on a surface of the semiconductor substrate,

ferroelectric capacitors corresponding in number to the cell transistors, provided above the semiconductor substrate, each of the ferroelectric capacitors has an upper electrode and a lower electrode electrically connected to one of a source diffusion layer and a drain diffusion layer of corresponding one of the cell transistors,

a plate line provided above the upper electrodes and electrically connected to the upper electrodes,

a reset transistor provided on the surface of the semiconductor substrate with one of a source diffusion layer and a drain diffusion layer electrically connected to the plate line,

a selection transistor provided on the surface of the semiconductor substrate with one of a source diffusion layer and a drain diffusion layer electrically connected to a bit line provided above the plate line,

a first active area formed on the surface of the semiconductor substrate to cross gate electrodes of the cell transistors in a plane and electrically connecting the other one of the source diffusion layer and the drain diffusion layer of the reset transistor to the other one of the source diffusion layer and the drain diffusion layer of the selection transistor, and

a plurality of second active areas formed on the surface of the semiconductor substrate to extend in a direction different from a first area extending direction, connected to the first active area in the plane, and electrically connecting the other one of the source diffusion layer and the drain diffusion layer of each one of the cell transistors to the other one of the source diffusion layer and the drain diffusion layer of the reset transistor.

76. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of cell transistors provided on the surface of the semiconductor substrate;

a first wiring layer provided above the cell transistors and electrically connected to one of a source diffusion layer and a drain diffusion layer of each of the plurality of cell transistors;

a plurality of ferroelectric capacitors provided above the first wiring layer, each of the ferroelectric capacitors having an upper electrode and a lower electrode electrically connected to the other of the source diffusion layer and the drain diffusion layer of each of the cell transistors;

a second wiring layer provided above the upper electrode and electrically connected to the upper electrode; and

a reset transistor provided on the surface of the semiconductor substrate with one of a source diffusion layer and a drain diffusion layer electrically connected to the second wiring layer and the other electrically connected to the first wiring layer.

77. The device according to claim 76, wherein the first wiring layer is a first local bit line, and the second wiring layer is a second local bit line.

78. The device according to claim 76, wherein the first wiring layer is a plate line, and the second wiring layer is a local bit line.

79. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of cell transistors provided on the surface of the semiconductor substrate;

a plurality of ferroelectric capacitors provided above the cell transistors, each of the ferroelectric capacitors having an upper electrode and a lower electrode electrically connected to one of a source diffusion layer and a drain diffusion layer of each of the cell transistors;

a plate line provided above the upper electrode and electrically connected to the upper electrodes of two adjacent ferroelectric capacitors;

a local bit line provided above the plate line and electrically connected to the other of the source

diffusion layer and the drain diffusion layer of each of the cell transistors;

a reset transistor provided on the surface of the semiconductor substrate with one of a source diffusion layer and a drain diffusion layer electrically connected to the plate line and the other electrically connected to the local bit line; and

a selection transistor provided on the surface of the semiconductor substrate with one of a source diffusion layer and a drain diffusion layer electrically connected to a bit line provided above the local bit line and the other electrically connected to the local bit line.